WHAT IS CLAIMED IS:

1. A High Performance Computing (HPC) node comprising:

a motherboard;

a switch comprising eight or more ports, the switch integrated on the motherboard; and

at least two processors operable to execute an HPC job, each processor communicably coupled to the integrated switch and integrated on the motherboard.

2. The HPC node of Claim 1, each processor coupled to the integrated switch through a Host Channel Adapter (HCA).

3. The HPC node of Claim 2, each processor further coupled to the integrated switch through a Hyper Transport/PCI bridge.

4. The HPC node of Claim 1, the processors communicably coupled via a Hyper Transport link.

5. The HPC node of Claim 1, each processor communicably coupled to the integrated switch through a North Bridge.

6. The HPC node of Claim 1, the integrated switch operable to communicate I/O messages at a bandwidth substantially similar to power of the processors.

7. The HPC node of Claim 1, the integrated switch comprising an Infiniband switch.

8. The HPC node of Claim 1, the integrated switch operable to:

communicate a first message from a first of the two or more processors; and

communicate a second message from a second of the two or more processors, the first and second message communicated in parallel.

9. A High Performance Computing (HPC) system comprising a plurality of interconnected HPC nodes, each node comprising:

a motherboard;

a switch comprising eight or more ports, the switch integrated on the motherboard and operable to interconnect at least a subset of the plurality of nodes; and

at least two processors operable to execute an HPC job, each processor communicably coupled to the integrated switch and integrated on the motherboard.

10. The HPC system of Claim 9, the two or more processors on each node coupled to the integrated switch through a Host Channel Adapter (HCA).

11. The HPC system of Claim 10, the two or more processors on each node further coupled to the integrated switch through a Hyper Transport/PCI bridge.

12. The HPC system of Claim 9, the two or more processors on each node communicably inter-coupled via a Hyper Transport link.

13. The HPC system of Claim 9, the two or more processors on each node communicably coupled to the integrated switch through a North Bridge.

14. The HPC system of Claim 9, the integrated switch of each node operable to communicate I/O messages at a bandwidth substantially similar to power of the processors.

15. The HPC system of Claim 9, the integrated switch of each node comprising an Infiniband switch.

16. The HPC system of Claim 9, the plurality of HPC nodes arranged in a topology, the topology enabled by the integrated fabric of each node.

17. The HPC system of Claim 16, the topology comprising a hypercube.

18. The HPC system of Claim 16, the topology comprising a folded topology.

19. The HPC system of Claim 9, a first node of the plurality of nodes interconnected to a second node of the plurality of nodes along an X axis, a third node of the plurality of nodes along a Y axis, a fourth node of the plurality of nodes along a Z axis, and a fifth node along a diagonal axis.

20. The HPC system of Claim 19, the connection between the first node and the fifth node operable to reduce message jumps among the plurality of nodes.

21. A method for forming an HPC node, comprising:

providing a motherboard;

integrating a switch with the motherboard;

integrating at least two processors with the motherboard; and

coupling each processor with the integrated switch.

22. The method of Claim 21, wherein coupling each processor with the integrated switch comprises coupling each processor to the integrated switch through a Host Channel Adapter (HCA).

23. The method of Claim 22, wherein coupling each processor with the integrated switch comprises coupling each processor to the integrated switch through a Hyper Transport/PCI bridge.

24. The method of Claim 21, further comprising coupling the processors via a Hyper Transport link.

25. The method of Claim 21, wherein coupling each processor with the integrated switch comprises coupling each processor communicably to the integrated switch through a North Bridge.

26. The method of Claim 21, the integrated switch operable to communicate I/O messages at a bandwidth substantially similar to power of the processors.

27. The method of Claim 21, the integrated switch comprising an Infiniband switch.